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Online: WPI, INSPEC, COMPUTER

(54) Flash memory with redundancy

(57) A repair circuit for replacing failed cells of main memory cell arrays with spare cells. The flash memory device comprises a main memory cell array 1, a redundancy cell block 2, a redundancy row decoder 3, a row decoder 4, a column decoder, a flag bit cell block 9, a flag cell transfer gate Q1, a main sense amplifier 7 and a flag sense amplifier 8.

FIG. 2

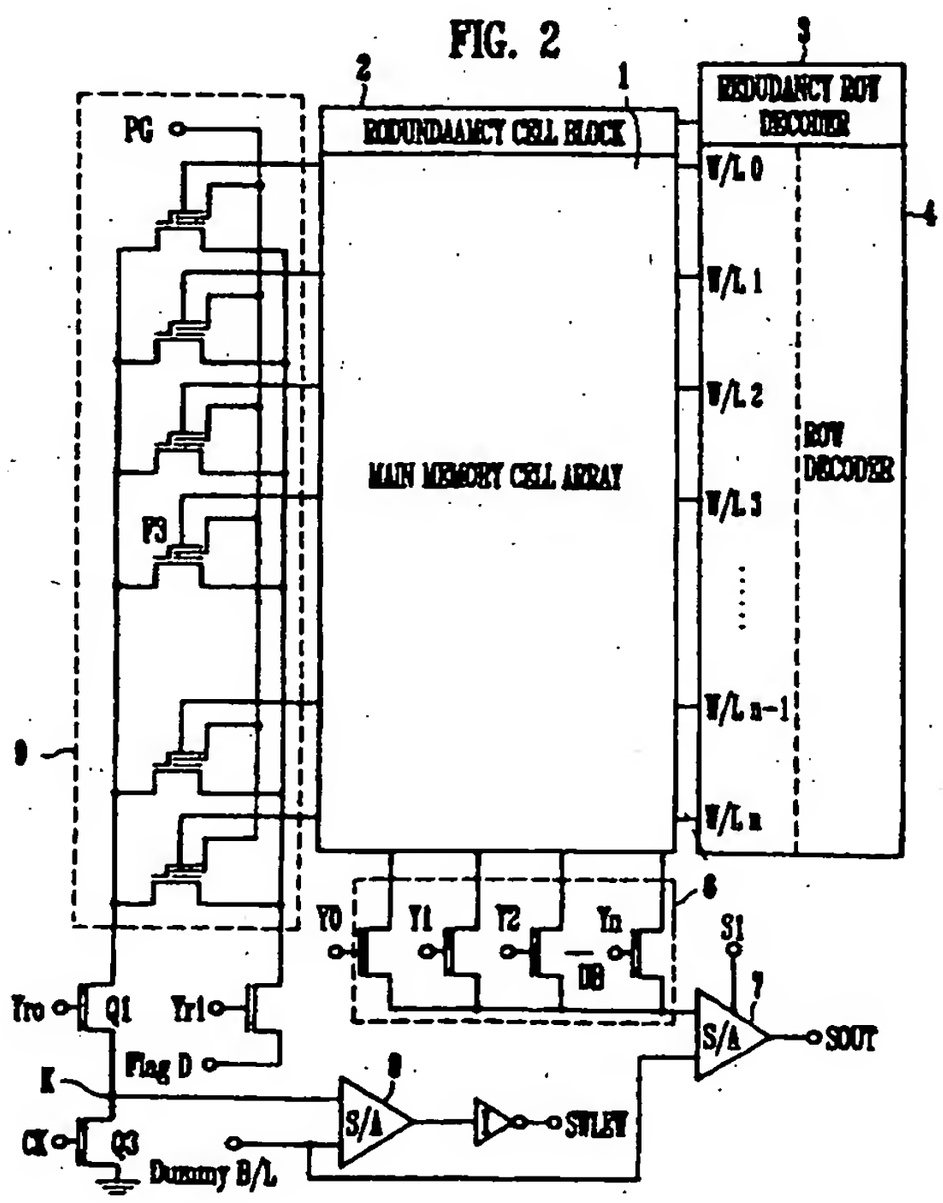

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FIG. 1 (PRIOR ART)

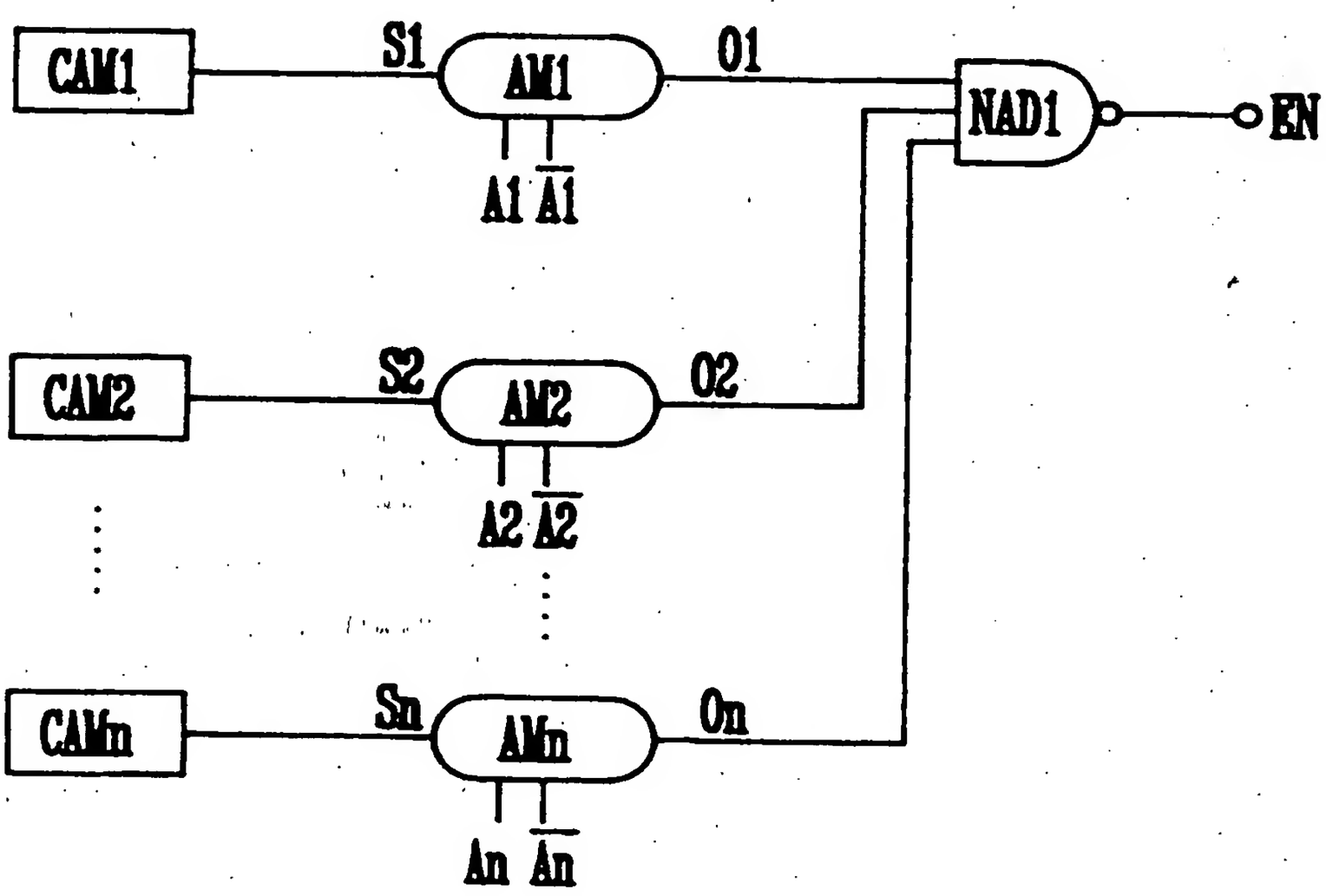


FIG. 2

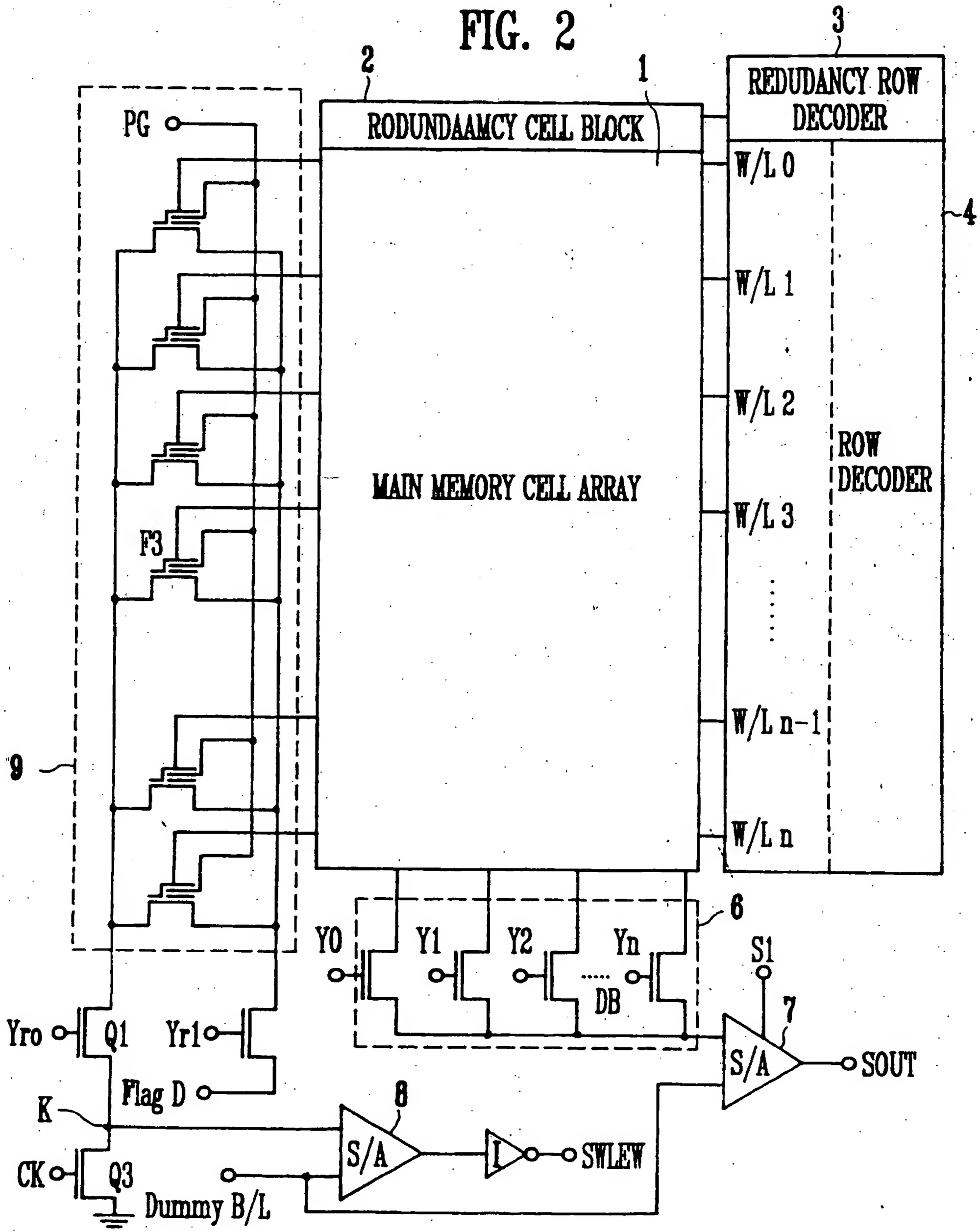

2
1
3
REDUDANCY ROW DECODER
RODUNDAAMCY CELL BLOCK
PG
W/L 0
4
W/L 1
W/L 2
ROW DECODER
MAIN MEMORY CELL ARRAY
F3
W/L 3
W/L n-1
9
W/L n
6
Y0
Y1
Y2
Yn
DB
S1
7
Yro
Q1
Yr1
S/A
SOUT
Flag D
8
K
S/A
I
SWLEW
CK
Q3
Dummy B/L

FIG. 3

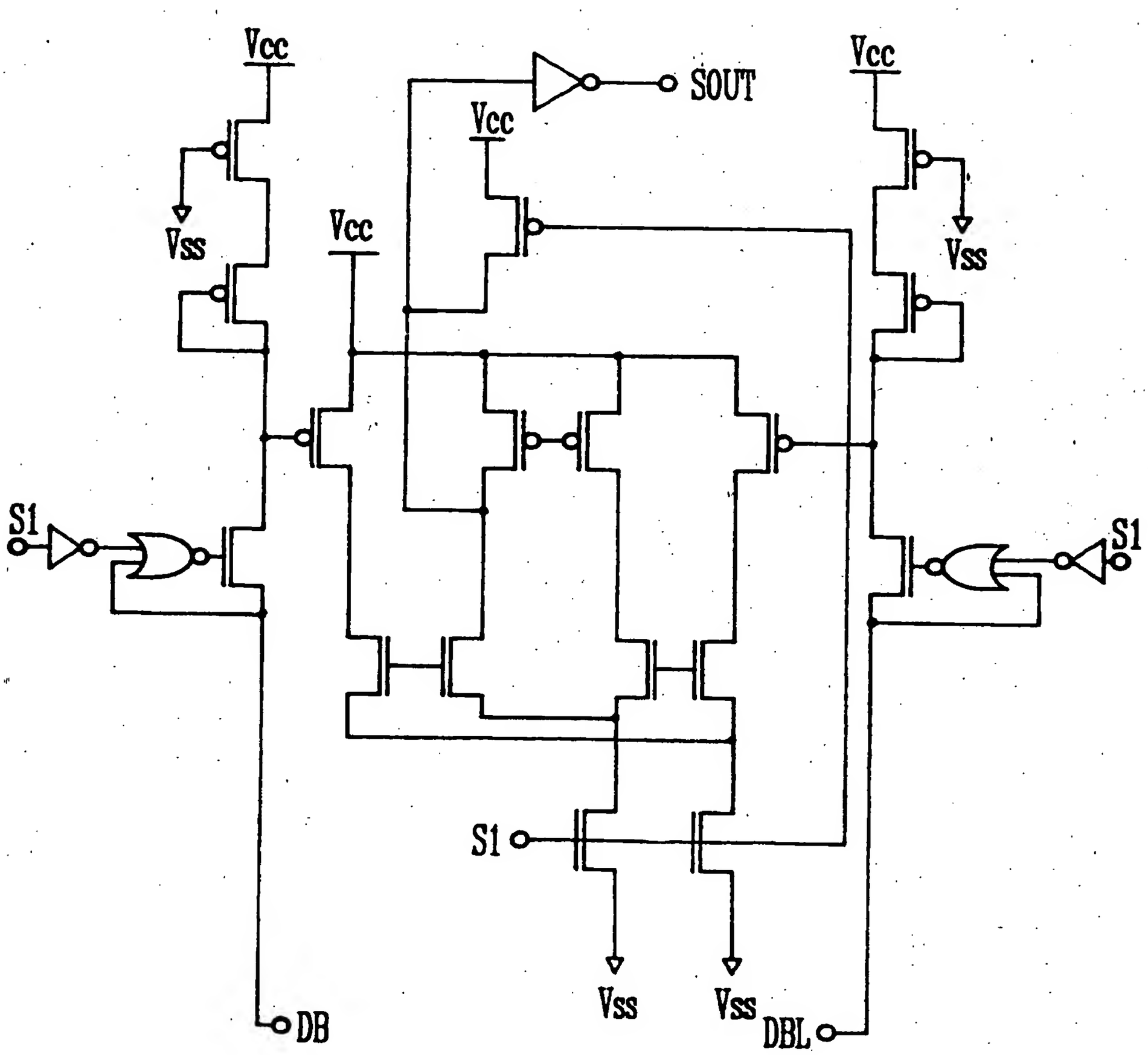


FIG. 4

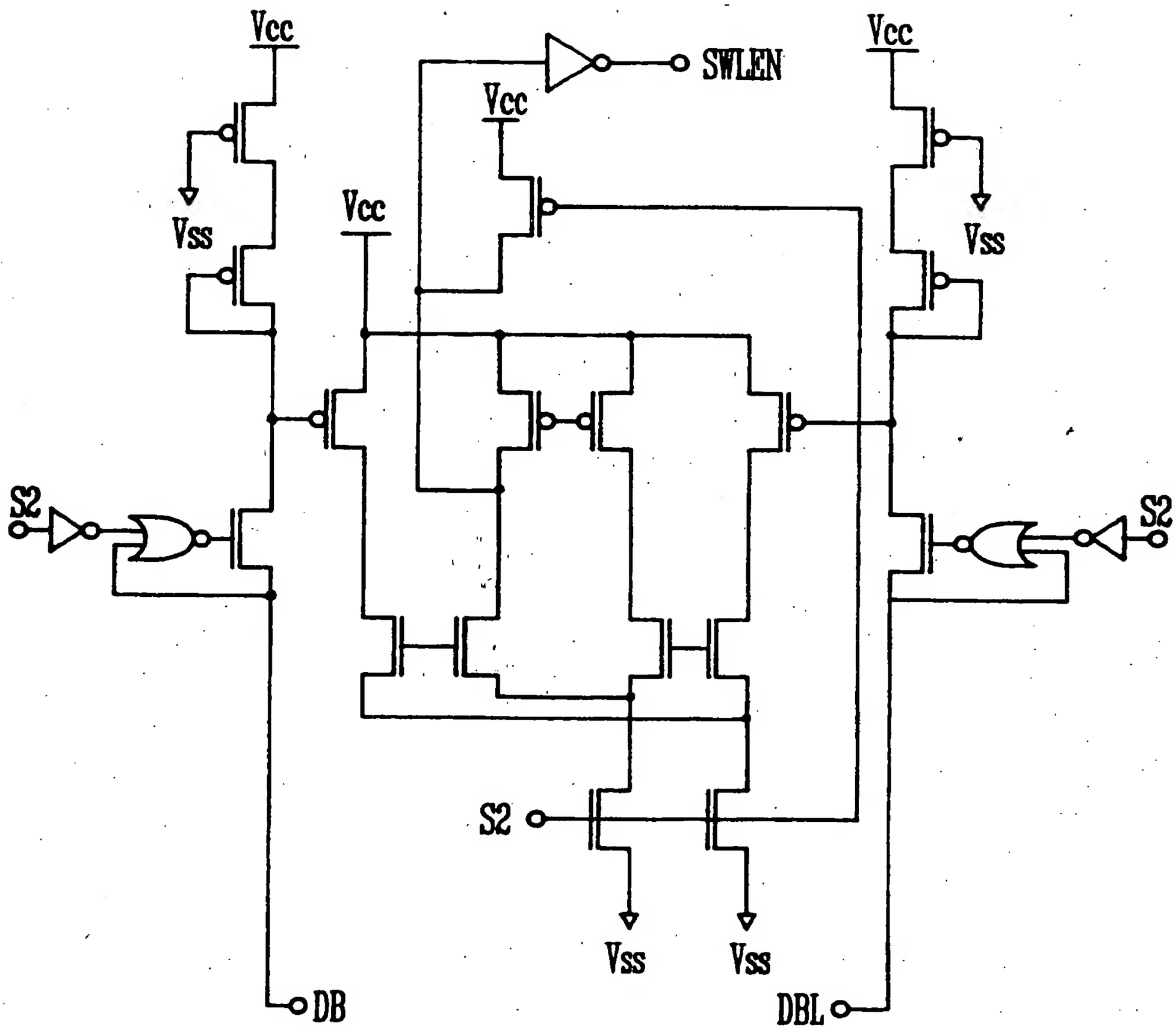
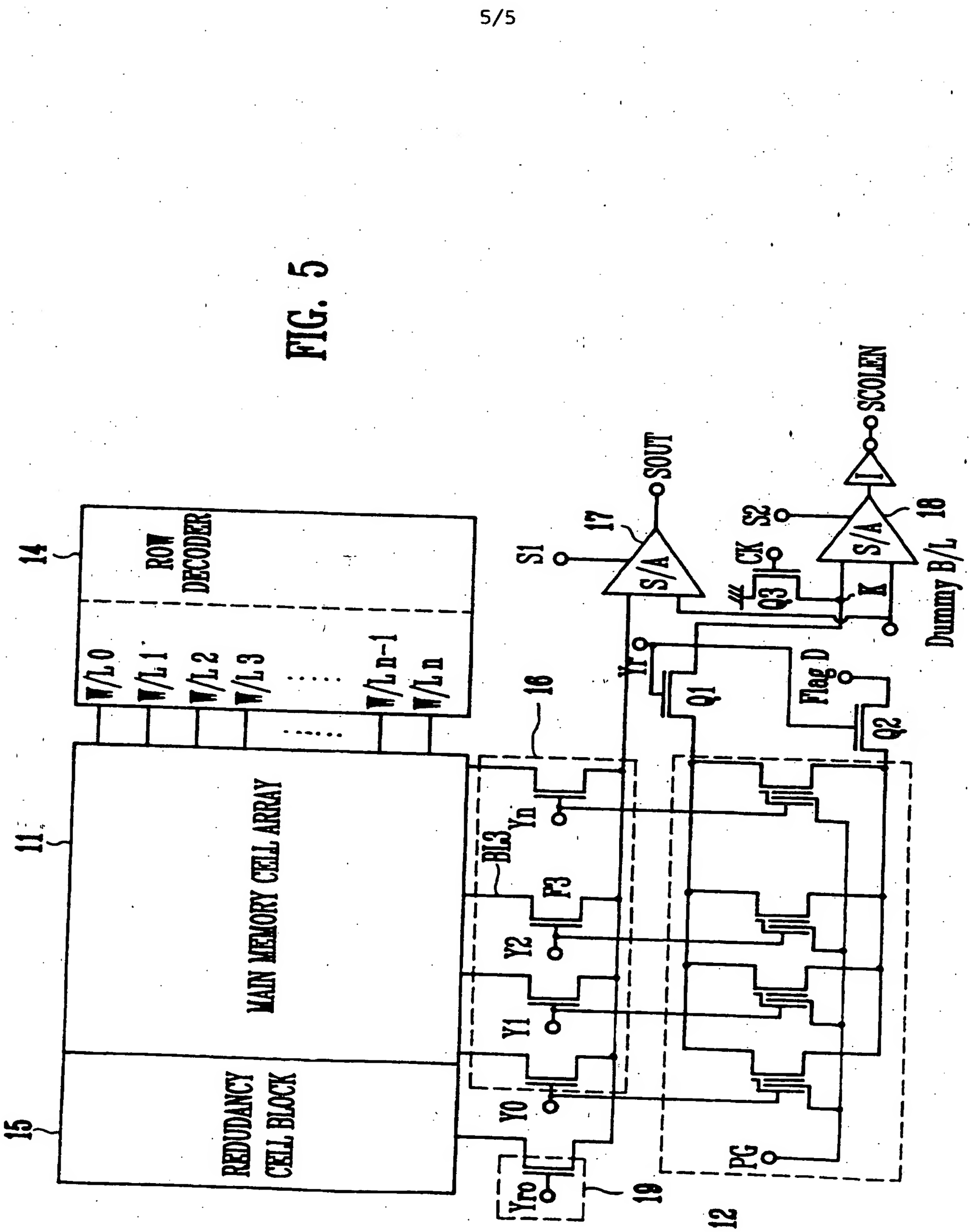


FIG 5


14
ROW DECODER
W/L 0
W/L 1
W/L 2
W/L 3
W/L n-1
W/L n
11
MAIN MEMORY CELL ARRAY
15
REDUDANCY CELL BLOCK
16
BL3
Yn
Y3
Y2
Y1
Y0
Yre
19
12
17
S/A
SOUT
S1
18
S/A
SCOLEN
S2
CK
Q3
K
Dummy B/L
Flag D
Q1
Q2
PC

FLASH MEMORY DEVICE

The present invention relates to a flash memory device, and more particularly to a flash memory device which allows a defect cell occurred in a main memory cell to be repaired.

Generally, it is said that what we call a redundancy cell is a spare cell which is added to replace a fail cell so as to improve the throughput of the device when the fail cell occurs in a main memory cell.

FIG.1 is a block diagram for explaining a conventional flash memory device, in which a plurality of CAMs(content addressable memories ; CAM1 to CAMn) are consisted in a form of latch on a address' base. Address matching circuits **AM1** to **AMn** determine which address is a fail address in response to the output data **S1** to **Sn** from the CAMs (CAM1 to CAMn). The output data **01** to **On** from the address matching circuits **AM1** to **AMn** generate an enable signal **EN** for driving a redundancy cell array(not shown) through a NAND gate NAND1. That is, it generates an enable signal **EN** for driving a redundancy cell array by sensing the cell on which a decision is given as fail.

The conventional repair circuit requires a additional logic circuit

because a row decoder has to enable a redundancy cell block immediately. In other words, the conventional repair circuit has a problem of a complicated structure and therefore a large chip area because it uses a CAM circuit consisted in a form of latch on a address' basis, an address matching circuit to which the output data from the CAM circuit is input, and a NAND gate to which the output data from the address matching circuit is input.

Accordingly, it is an object of the present invention to provide a flash memory device which can overcome the above mentioned problem.

To achieve the above object, an flash memory device comprising:

a main cell array having a plurality of word lines and a plurality of bit lines;

a column decoder for selecting any one of the bit lines;

a row decoder for selecting any one of the word lines;

a redundancy cell block connected between the plurality of bit lines and a plurality of spare word lines;

a flag bit cell block coupled to the plurality of word lines, for storing whether the word line is failed or not;

a flag sense amplifier coupled to a dummy bit line connected to a reference cell and the flag bit cell block;

a redundancy row decoder for selecting the spare word lines in

response to the output signal of the flag sense amplifier; and

a main sense amplifier coupled to the dummy bit line and the column decoder.

For fuller understanding of the nature and object of the invention, reference should be had to the following detailed description taken in conjunction with the accompanying drawings in which:

FIG.1 is a block diagram of a conventional repair device;

FIG.2 illustrates a circuit diagram of a flash memory device having a repair circuit according to a first embodiment of the present invention;

FIG.3 is a detailed view of a main sense amplifier shown in FIG.1;

FIG.4 is a detailed view of a flag sense amplifier shown in FIG.1; and

FIG.5 illustrates a block diagram of a flash memory device according to a second embodiment of the present invention.

Similar reference characters refer to similar parts in the several views of the drawings.

Below, the present invention will be described in detail by reference to the accompanying drawings.

FIG.2 illustrates a circuit diagram of a flash memory device with a

repair circuit according to a first embodiment of the present invention.

A flag bit cell block 9 is positioned within a guard ring of a main memory cell array 1. The flag bit cell block 9 is consisted of a plurality of flash memory cells. Each control gate electrode of the flash memory cells is connected to a program terminal PG. A select gate electrode of each of the flash memory cells is connected to each of word lines W/L0, W/L1, ... W/Ln-1, W/Ln. A source electrode of each of the flash memory cells is grounded via a flag bit transfer transistor Q1, a node K and transistor Q3. The flag bit transfer transistor Q1 is turned on in response to a flag bit decoder signal Yro. The transistor Q3 is turned on in response to a clock signal CK. The drain electrode of each of the flash memory cells is connected to a flag terminal (Flag-D) through a flag bit transfer transistor Q2.

The node K is connected to one of the input terminals of the flag sense amplifier 8. Another input terminal of the flag sense amplifier 8 is connected to a dummy bit line(Dummy B/L) to which a reference cell is connected. The output terminal from the flag sense amplifier 8 is connected to an inverter I. A redundancy row decoder 3 is enabled by the output of the inverter I.

A row decoder 4 is connected to the word lines W/L0, W/L1, ... W/Ln-1, W/Ln in the main memory cell 1. The redundancy cell block 2 is connected between the bit line of the main memory cell array 1 and a spare word line. The redundancy cell block 2 is enabled by the redundancy

row decoder 3. A column decoder 6 is connected to the bit line of the main memory cell array 1. The column decoder 6 is connected to one of the input terminals of the main sense amplifier 7. Another input terminal of the main sense amplifier 7 is connected to the dummy bit line.

For example, the case in which a word line WLi selected by the row decoder 4 is failed will be explained as follows.

The transistors **Q1** and **Q3** are turned on by the clock signal **CK** and the flag bit decoder signal **Yro**. A program voltage is applied to the control gate electrode of the flash memory cell **F3** through the program terminal **PG**. As the transistor **Q2** is turned on by a flag bit decoder signal **Yr1**, a voltage of 5 volt is for example supplied to the drain electrode of the flash memory cell **F3**. Thus the flash memory cell **F3** is programmed.

Thereinafter, when a read operation is performed, the transistor **Q3** is turned off while the transistors **Q1** and **Q2** are turned on. The flag terminal **(Flag D)** is grounded. The flag sense amplifier 8 outputs information stored on the flash memory cell **F3** by sensing it. As the redundancy row decoder 3 is enabled in response to the output SWLEW of the inverter 18, the redundancy cell block 2 is selected. Information stored on the cell of the redundancy cell block 2 is output by the main sense amplifier 7 in response to column decoder signals **Y0** to **Yn**.

FIG.3 is a detailed view of a main sense amplifier shown in FIG.1, which senses the cell data of the main memory cell block through a data

bit line DB in response to the input of the sense amplifier enable signal S1. Then the dummy bit line DBL becomes a low voltage level.

FIG.4 is a detailed view of a flag sense amplifier shown in FIG.1, which senses the cell data of the redundancy memory cell block through a dummy bit line DBL in response to the input of the sense amplifier enable signal S2. Then the data bit line DB becomes a low voltage level.

FIG.5 illustrates a block diagram of a flash memory device with a repair circuit according to a second embodiment of the present invention.

A flag bit cell block 12 is positioned within a guard ring of the main memory cell array 1. The flag bit cell block 12 is consisted of a plurality of flash memory cells. A control gate electrode of each of the flash memory cells is connected to a program terminal PG. A select gate electrode of each of the flash memory cells is connected to each of the gate electrode of each of the transistors in a column decoder 16. A source electrode of each of the flash memory cells is grounded via a flag bit transfer transistor Q1, a node K and transistor Q3. The flag bit transfer transistor Q1 is turned on in response to a flag bit decoder signal Yr. The transistor Q3 is turned on in response to a clock signal CK. The drain terminal of each of the flash memory cells is connected to a flag terminal (Flag-D) through a flag bit transfer transistor Q2 which is turned on in response to the flag bit decoder signal Yr.

The node K is connected to one of the input terminals of the flag sense amplifier 18. Another input terminal of the flag sense amplifier 18 is

connected to a dummy bit line (Dummy B.L) to which a reference cell is connected. The output terminal of the flag sense amplifier 18 is connected to an inverter I. A redundancy column decoder 19 is enabled by the output SCOLEN of the inverter.

A row decoder 14 is connected to the word lines W/Lo, W/L1, ... ; W/Ln-1, W/Ln in the main memory cell 1. The redundancy cell block 2 is connected between the word line of the main memory cell array 1 and a spare bit line. The redundancy cell block 2 is enabled by the redundancy column decoder 19. A column decoder 16 is connected to the bit line of the main memory cell array 1. The column decoder 16 is connected to one of the input terminals of the main sense amplifier 17. Another input terminal of the main sense amplifier 17 is connected to the dummy bit line.

For example, the case in which a bit line BL3 selected by the column decoder 16 is a failed will be explained as follows.

The transistors Q3 and Q1 are turned on by the clock signal CK and the flag bit decoder signal Yr. A program voltage is applied to the control gate electrode of the flash memory cell F3 through the program terminal PG. As the transistor Q2 is also turned on by a flag bit decoder signal Yr, a voltage of 5 volt is for example supplied to the drain electrode of the flash memory cell F3. Thus the flash memory cell F3 is programmed.

Thereinafter, when a read operation is performed, the transistor Q3 is turned off while the transistors Q1 and Q2 are turned on. The flag

terminal **(Flag D)** is grounded. The flag sense amplifier 18 outputs information stored on the flash memory cell F3 by sensing it. As the redundancy column decoder 19 is enabled in response to the output SCOLEN of the inverter I, a spare bit line in the redundancy cell block 2 is selected.

As mentioned above, the flash memory device of the present invention has an outstanding effect which can not only improve the repair efficiency but reduce the chip size, by positioning a flag bit cell block capable of programming a repair information within a guard ring of the memory cell array and replacing a fail word line or a bit line with a spare word line or a spare bit line in response to the repair information.

The foregoing description, although described in its preferred embodiment with a certain degree of particularity, is only illustrative of the principles of the present invention. It is to be understood that the present invention is not to be limited to the preferred embodiments disclosed and illustrated herein. Accordingly, all expedient variations that may be made within the scope of the present invention are to be encompassed as further embodiments of the present invention.

CLAIMS:

1. A flash memory device comprising:

a main cell array having a plurality of word lines and a plurality of bit lines;

a column decoder for selecting any one of said bit lines;

a row decoder for selecting any one of said word lines;

a redundancy cell block connected between said bit lines and a plurality of spare word lines;

a flag bit cell block coupled to said word lines, for storing whether any one word line of said word lines is failed or not;

a flag sense amplifier coupled to a dummy bit line connected to a reference cell and said flag bit cell block;

a redundancy row decoder for selecting said spare word lines in response to an output signal of the flag sense amplifier; and

a main sense amplifier coupled to said dummy bit line and said column decoder.

2. The flash memory device claimed in Claim 1 wherein said flag bit cell block is positioned within a guard ring of the main cell array.

3. The flash memory device claimed in Claim 1 wherein said flag bit cell block is consisted of flash memory cells.

4. A flash memory device comprising:

a main cell array having a plurality of word lines and a plurality of bit lines;

a column decoder for selecting any one of said bit lines;

a row decoder for selecting any one of said word lines;

a redundancy cell block connected between said word lines and a plurality of spare bit lines;

a flag bit cell block coupled to said column decoder, for storing whether any one bit line of said bit lines is failed or not;

a flag sense amplifier coupled to a dummy bit line which is connected to a reference cell and said flag bit cell block;

a redundancy column decoder for selecting said spare bit lines in response to an output signal of said flag sense amplifier; and

a main sense amplifier coupled to said dummy bit line and said column decoder.

5. The flash memory device claimed in Claim 4 wherein said flag bit cell block is positioned within a guard ring of the main cell array.

6. The flash memory device claimed in Claim 4 wherein said flag bit cell block is consisted of flash memory cells.

7. A flash memory device substantially as hereinbefore described with reference to Figures 2 to 4 or Figure 5.

The Patent Office

Application No: GB 9626913.9
Claims searched: All

Examiner: Matthew Gillard
Date of search: 18 February 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): G4A AEF

Int Cl (Ed.6): G06F 11/20

Other: On-line: COMPUTER, INSPEC, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	EP 0511560 A2 (I. B. M.).	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.